UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,676	07/21/2003	Tarik Hammadou	CML00878AC	5080

7590 05/31/2005

Daniel K. Nichols
Motorola, Inc. - Law Department
1303 E. Algonquin Road
Schaumburg, IL 60196

EXAMINER	
KANG, DONGHEE	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/623,676	HAMMADOU ET AL.	
	Examiner	Art Unit	
	Donghee Kang	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 12-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 & 12-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims **1-10, 12-17, & 19-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US 2003/0042587) in view of He et al. (US 6,462,365).

Re claims 1 & 21, Lee teaches a sensor array having a plurality of programmable cells, each of the cells comprising (Fig.25):

a programmable module (102); and a sensor element (701) operatively coupled to the programmable module, wherein the programmable module is programmable to perform logic functions and in use the sensor element provides a signal to the programmable module, the signal being dependent upon variations in an ambient condition monitored by the sensor element. Lee teaches module 102 is a microprocessor but a configurable logic block. He et al. teach in Fig.10 the processor circuit 1105 is capable of executing a set of programmed instruction to carry functions of integrated circuit and is a conventional microprocessor, DSP or **FPGA** (Col.5, lines 50-56). FPGA has a large number of configurable logical blocks (CLBS). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute microprocessor of Lee with FPGA as taught by He since

microprocessor and FPGA would work equally well as a programmable module for performing logic function.

Re claims 2 & 22, Lee teaches a programmable sensor array further including analogue module (101) operatively coupling the programmable module to the sensor element.

Re claim 3, Lee teaches the sensor element is an image sensor element.

Re claim 4, Lee teaches the image sensor element is pixel element.

Re claim 5, Lee teaches the sensor element and programmable module are in a stacked relationship.

Re claim 6, Lee teaches the sensor element, programmable module and analogue module are in stacked relationship.

Re claims 7 & 23, Lee teaches the analogue module is sandwiched between the sensor element and programmable module.

Re claim 8, Lee teaches the sensor element is formed on an upper semiconductor substrate.

Re claim 9, Lee teaches the programmable module is formed on a lower semiconductor substrate.

Re claim 10, Lee teaches the analogue module is formed on an intermediate semiconductor substrate sandwiched between the upper semiconductor substrate and lower semiconductor substrate.

Re claim 11, Lee teaches the programmable module comprises configurable logic blocks.

Re claims 13-16, Lee teaches in plan view the sensor element is directly aligned with the programmable module and the analogue module.

Re claim 17, Lee teaches the cells are operatively coupled to input-output ports thereby allowing communication of the sensor array with external electronic circuitry.

Re claims 19-20, Lee teaches the analogue module includes a differential amplifier or comparator.

3. Claims **1-3, 7, 12, 18 & 21-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Stam et al. (US 5,837,994) in view of He et al. (US 6,462,365).

Re claims 1 & 21, Stam et al. teach a programmable sensor array having a plurality of programmable cells, each of the cells comprising (Fig.5):

A programmable module (204); and a sensor element (201) operatively coupled to the programmable module, wherein the programmable module is programmable to perform logic functions and in use the sensor element provides a signal to the programmable module, the signal being dependent upon variations in an ambient condition monitored by the sensor element. Stam teaches module 204 is a microprocessor but a configurable logic block. He et al. teach in Fig.10 the processor circuit 1105 is capable of executing a set of programmed instruction to carry functions of integrated circuit and is a conventional microprocessor, DSP or **FPGA** (Col.5, lines 50-56). FPGA has a large number of configurable logical blocks (CLBS). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute microprocessor of Stam with FPGA as taught by He since

microprocessor and FPGA would work equally well as a programmable module for performing logic function.

Re claims 2 & 22, Stam et al. teach a programmable sensor array further including analogue module (202) operatively coupling the programmable module to the sensor element.

Re claim 3, Stam et al. teach the sensor element is an image sensor element.

Re claims 7 & 23, Stam et al. teach the analogue module is sandwiched between the sensor element and programmable module.

Re claim 12, Stam et al. teach the programmable module forms part a field programmable logic array.

Re claim 18, Stam et al. teach the analogue module is an analogue to digital converter.

Response to Arguments

4. Applicant's arguments with respect to claims 1-10 & 12-23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 571-272-1656. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Donghee Kang
Primary Examiner
Art Unit 2811

dhk